



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Eliyahou Harari et al.
Title: Multi-State Non-Volatile Integrated Circuit Memory Systems That
Employ Dielectric Storage Elements
Application No.: 10/002,696 Filing Date: October 31, 2001
Examiner: Weiss, Howard Group Art Unit: 2814
Docket No.: SNDK.272US0 Conf. No.: 4652

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97 and 1.98, Applicants call the documents listed on the enclosed Form PTO-1449 to the Examiner's attention in this patent application. Copies of the documents listed on the accompanying Form PTO-1449 are enclosed.

Citation of these documents shall not be construed as (1) an admission that the documents are prior art with respect to the invention or inventions claimed in this application, (2) a representation that a search has been made (other than as indicated by any cited document), or (3) an admission that the cited information is, or is considered to be, material to patentability as defined in § 1.56(b).

This information disclosure statement is submitted under 37 C.F.R. § 1.97(b) and consequently no fee should be required. The Commissioner is authorized, however, to charge

Attorney Docket No.: SNDK.272US0

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any fee that may be required, or to credit any overpayment, against Deposit Account No. 502664, as set forth in the accompanying Transmittal Letter.

EXPRESS MAIL
LABEL NO.:

EV437667615US

Respectfully submitted,



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April 6, 2004

Date

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U.S. Department of Commerce, Patent and Trademark				Atty. Docket No.		Application No.	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				SNDK.272US0		10/002,696	
				Applicants		Conf. No.	
(Use several sheets if necessary)				Eliyahou Harari et al.		4652	
				Filing Date		Art Group	
				October 31, 2001		2814	

U.S. Patent Documents							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	13	6,181,597	1/30/2001	Nachumovsky			
	14	5,168,334	12/1/1992	Mitchell et al.			
	15	6,101,125	8/8/2000	Gorman			

U.S. Published Patent Application Documents							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	16	2003/0080372A1	5/1/2003	Mikolajick			
	17	2003/0081456A1	5/1/2003	Mikolajick			
	18	2002/0130350A1	9/19/2002	Shin et al.			
	19	2003/0081460A1	5/1/2003	Choi et al.			
	20	2003/0016561A1	1/23/2003	Lee et al.			
	21	2003/0030097A1	2/13/2003	Lee et al.			

Foreign Patent Documents								
							Translation	
		Document	Date	Country	Class	Subclass	Yes	No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)		

Examiner	Date Considered
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

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U.S. Patent Documents							
Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	1	6,552,387 B1	4/22/2003	Eitan			
	2	5,824,584	10/20/1998	Chen et al.			
	3	5,969,383	10/19/1999	Chang et al.			
	4	6,548,861 B2	4/15/2003	Palm et al.			
	5	6,313,503 B1	11/6/2001	Lee et al.			
	6	6,555,865 B2	4/29/2003	Lee et al.			
	7	6,677,200 B2	1/13/2004	Lee et al.			
	8	6,580,120 B2	6/17/2003	Haspeslagh			

U.S. Published Patent Application Documents							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	9	2003/0134476A1	7/17/2003	Roizin et al.			
	10	2003/0209754A1	11/13/2003	Haspeslagh			
	11	2002/0196665A1	12/26/2002	Kim			

Foreign Patent Documents								
							Translation	
		Document	Date	Country	Class	Subclass	Yes	No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)		
	12	Luc Haspeslagh, "Two Bit Non-Volatile Electrically Erasable and Programmable Memory Structure, a Process for Producing Said Memory Structure and Methods for Programming and Erasing Said Memory Structure", Provisional Application 60/296,618, filed June 7, 2001, priority claimed by US 6,580,120.

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